PSEUDO-RANDOM WAIT-STATE AND PSEUDO-RANDOM LATENCY COMPONENTS

Abstract of the Disclosure

5

Methods and apparatus are provided for testing logic, particularly arbitration logic on a programmable chip. Secondary components on a programmable chip are configured with delay mechanisms operable to pseudo-randomly delay responses to requests received using arbitration logic. Requests are typically generated by primary

10   components. The delay mechanisms can be used to test the ability of a programmable chip system to handle a variety of secondary component wait-state and latency characteristics. The delay mechanism can also be used to improve system performance.